

I²C bus extender

82B715

DESCRIPTION

The 82B715 is a bipolar integrated circuit intended for application in I²C bus systems.

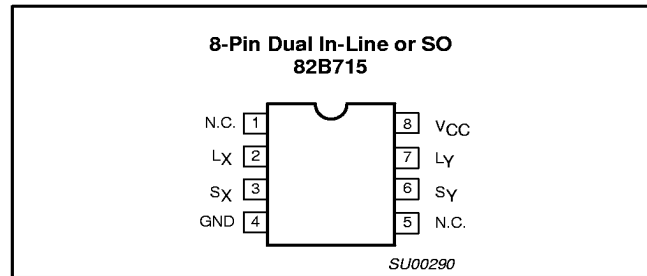
While retaining all the operating modes and features of the I²C system it permits extension of the practical separation distance between components on the I²C bus by buffering both the data (SDA) and the clock (SCL) lines.

The I²C bus capacitance limit of 400pF restricts practical communication distances to a few meters. Using one 82B715 at each end of longer cables reduces the cable loading capacitance on the I²C bus by a factor of 10 times and may allow the use of low cost general purpose wiring to extend bus lengths.

FEATURES

- Dual, bi-directional, unity voltage gain buffer
- I²C bus compatible
- Logic signal levels may include both supply and ground
- X10 impedance transformation
- Wide supply voltage range

PIN CONFIGURATIONS



PINNING

PIN	SYMBOL	FUNCTION
1	N.C.	
2	L _X	Buffered Bus, LDA or LCL
3	S _X	I ² C Bus, SDA or SCL
4	GND	Negative Supply
5	N.C.	
6	S _Y	I ² C Bus, SCL or SDA
7	L _Y	Buffered Bus, LCL or LDA
8	V _{CC}	Positive Supply

QUICK REFERENCE DATA

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.	MAX.	
V _{CC}	Supply voltage	4.5		12	V
I _{CC}	Quiescent current		16		mA
I _{line}	Output sink capability	30			mA
V _{in}	Input voltage range	0		V _{CC}	V
V _{out}	Output voltage range	0		V _{CC}	V
Z _{in} /Z _{out}	Impedance transformation	8	10	13	
T _{amb}	Temperature range	-40		+85	°C

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
8-pin plastic dual In-line package	P82B715P N	SOT97-1
8-pin plastic small outline package	P82B715T D	SOT96-1

NOTE:

1. For applications requiring, 3V operation and additional buffer performance, see P82B96 Data Sheet.

I²C bus extender

82B715

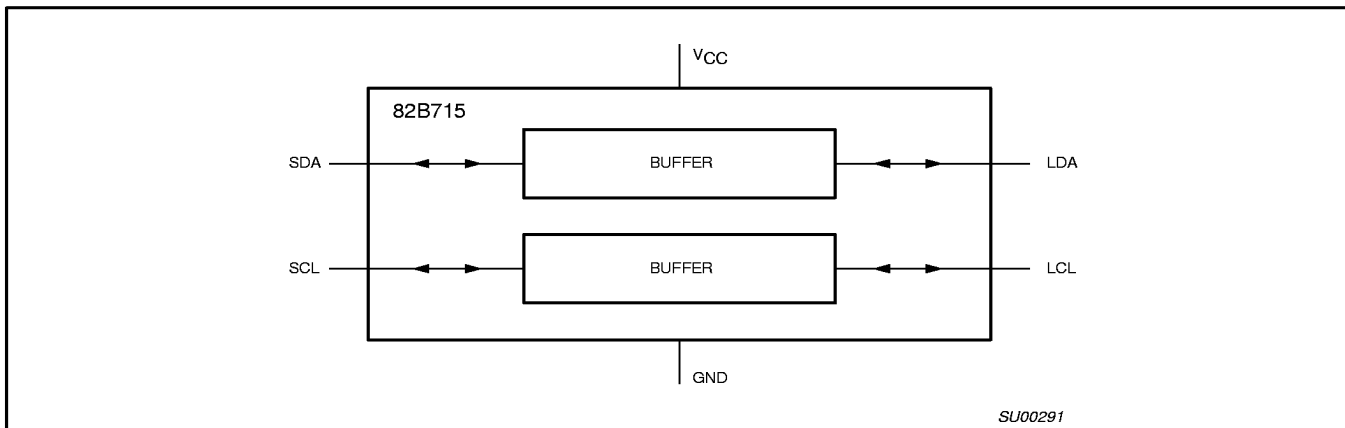


Figure 1. Block Diagram: 82B715

I²C bus extender

82B715

FUNCTIONAL DESCRIPTION

The 82B715 bipolar integrated circuit contains two identical buffer circuits which enable I²C and similar bus systems to be extended over long distances without degradation of system performance or requiring the use of special cables.

The buffer has an effective current gain of ten from I²C bus to Buffered bus. Whatever current is flowing out of the I²C bus side, ten times that current will be flowing into the Buffered bus side (see Figure 2).

As a consequence of this amplification the system is able to drive capacitive loads up to ten times the standard limit on the Buffered bus side. This current based buffering approach preserves the bi-directional, open-collector/open-drain characteristic of the I²C SDA/SCL lines.

To minimize interference and ensure stability, current rise and fall rates are internally controlled.

APPLICATION NOTES

By using two (or more) 82B715 ICs, a sub-system can be built which retains the interface characteristics of an I²C device so that it may be included in, or optionally added to, any I²C or related system.

The sub-system features a low impedance or "Buffered" bus, capable of driving large wiring capacities (see Figure 3).

I²C Systems

As with the standard I²C system, pull-up resistors are required to provide the logic HIGH levels on the Buffered bus. (Standard open-collector configuration of the I²C bus). The size and number of these pull-up resistors depends on the system.

If the buffer is to be permanently connected into the system, the circuit should be configured with only one pull-up resistor on the Buffered bus and none on the I²C bus.

Alternatively a buffer may be connected to an existing I²C system. In this case the Buffered bus pull-up will act in parallel with the I²C bus pull-up.

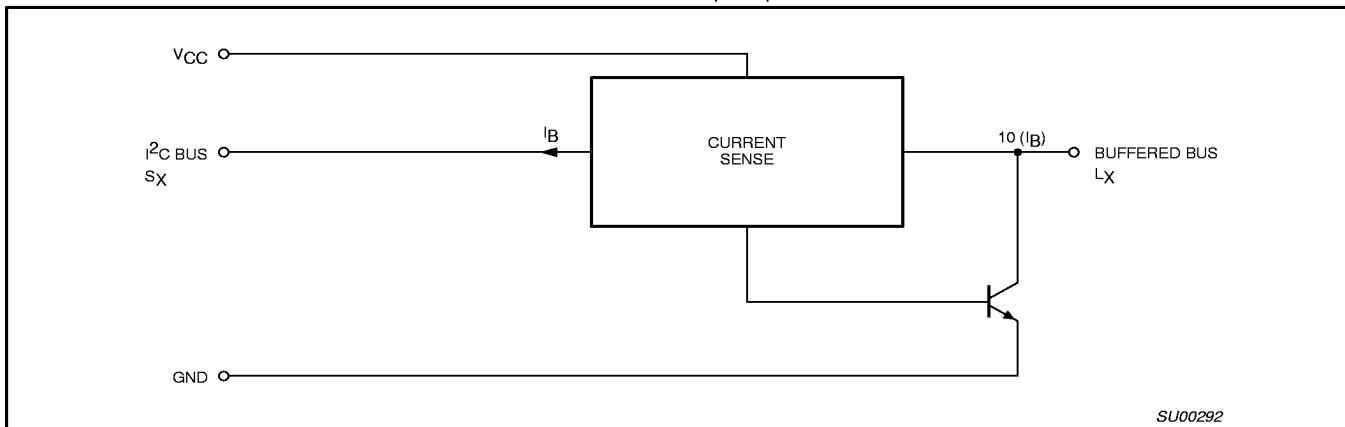


Figure 2. Equivalent Circuit: One Half 82B715

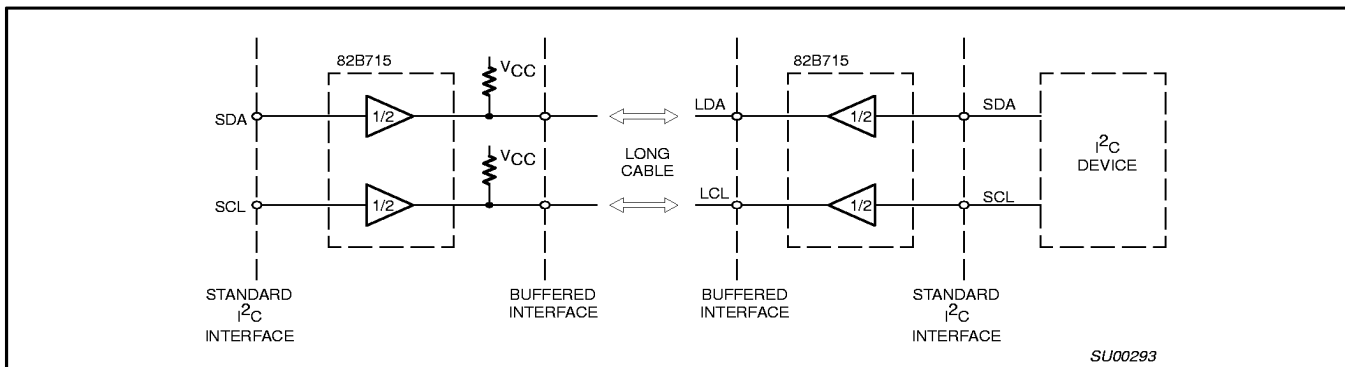


Figure 3. Minimum Sub-System with 82B715

I²C bus extender

82B715

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).
 Voltages with respect to pin GND (DIL-8 pin 4).

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN.	MAX.	
V _{CC} to GND	Supply voltage range V _{CC}	-0.3	+12	V
V _{bus}	Voltage range I ² C Bus, SCL or SDA	0	V _{CC}	V
V _{buff}	Voltage range Buffered Bus	0	V _{CC}	V
I	DC current (any pin)		60	mA
P _{tot}	Power dissipation		300	mW
T _{stg}	Storage temperature range	-55	+125	°C
T _{amb}	Operating ambient temperature range	-40	+85	°C

CHARACTERISTICS

At T_{amb} = +25°C and V_{CC} = 5 Volts, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.	MAX.	
Power Supply					
V _{CC}	Supply voltage (operating)	4.5	—	12	V
I _{CC}	Supply current	—	16	—	mA
I _{CC}	Supply current at V _{CC} = 12V	—	22	—	mA
I _{CC}	Supply current, both I ² C inputs LOW, both buffered outputs sinking 30mA.	—	28	—	mA
Drive Currents					
I _{Sx} , I _{Sy}	Output sink on I ² C bus V _{Sx} , V _{Sy} LOW = 0.4V V _{Lx} , V _{Ly} LOW on Buffered bus = 0.3V	3	—	—	mA
I _{Lx} , I _{Ly}	Output sink on Buffered bus V _{Lx} , V _{Ly} LOW = 0.4V V _{Sx} , V _{Sy} LOW on I ² C bus = 0.3V	30	—	—	mA
Input Currents					
I _{Sx} , I _{Sy}	Input current from I ² C bus when I _{Lx} , I _{Ly} sink on Buffered bus = 30mA	—	—	3	mA
I _{Lx} , I _{Ly}	Input current from Buffered bus when I _{Sx} , I _{Sy} sink on I ² C bus = 3mA	—	—	3	mA
I _{Lx} , I _{Ly}	Leakage current on Buffered bus V _{Lx} , V _{Ly} = V _{CC} , and V _{Sx} , V _{Sy} = V _{CC}	—	—	200	μA
Impedance Transformation					
Z _{in} /Z _{out}	Input/Output impedance	8	10	13	

Pull-Up Resistance Calculation

In calculating the pull-up resistance values, the gain of the buffer introduces scaling factors which must be applied to the system components. Viewing the system from the Buffered bus, all I²C bus capacitances have effectively 10 times their I²C bus value.

In practical systems the pull-up resistance is determined by the rise time limit for I²C systems. As an approximation this limit will be satisfied if the time constant (product of the net resistance and net capacitance) of the total system is set to 1 microsecond.

The total time constant may either be set by considering each bus node individually (i.e., the I²C nodes, and the Buffered bus node) and choosing pull-up resistors to give time constants of 1 microsecond for each node; or by combining the capacitances into an equivalent capacitive loading on the Buffered bus, and

calculating the Buffered bus pull-up resistor required by this equivalent capacitance.

For each separate bus the pull-up resistor may be calculated as follows:

$$R = \frac{1 \mu \text{sec}}{C_{\text{device}} + C_{\text{wiring}}}$$

Where: C_{device} = sum of device capacitances connected to each bus,

and C_{wiring} = total wiring and stray capacitance on each bus.

If these capacitances are not known then a good approximation is to assume that each device presents 10pF of load capacitance and 10pF of wiring capacitance.

I²C bus extender

82B715

The capacitance figures for one or more individual I²C bus nodes should be multiplied by a factor of 10 times, and then added to the Buffered bus capacitance. Calculation of a new Buffered bus pull-up resistor will allow this single pull-up resistor to act for both the included I²C bus nodes and the Buffered bus. Thus it is possible to combine some or all of these separate pull-up resistors into a single resistor on the Buffered bus (the value of which is calculated from the sum of the scaled capacitances on the Buffered bus). If the buffer is to be permanently connected into the system then all the separate pull-up resistors should be combined. But if it is to be connected by adding it onto an existing system, then only those on the additional I²C bus system can be combined onto the Buffered bus if the original system is required to be able to still operate on a stand-alone basis.

A further restriction is that the maximum pull-up current, with the bus LOW, should not exceed the I²C bus specification maximum of 3mA, or 30mA on the Buffered bus. The following formula applies:

$$30\text{mA} > \frac{V_{CC} - 0.4}{R_p}$$

Where: R_p = scaled parallel combination of all pull-up resistors.

If this condition is met, the fall time specifications will also be met.

Figure 4 shows typical loading calculations for the expanded I²C bus.

Sx, Sy, I²C Bus, SDA or SCL

Because the two buffer circuits in the 82B715 are identical either input pin can be used as the I²C Bus SDA data line, or the SCL clock line.

Lx, Ly, Buffered Bus, LDA or LCL

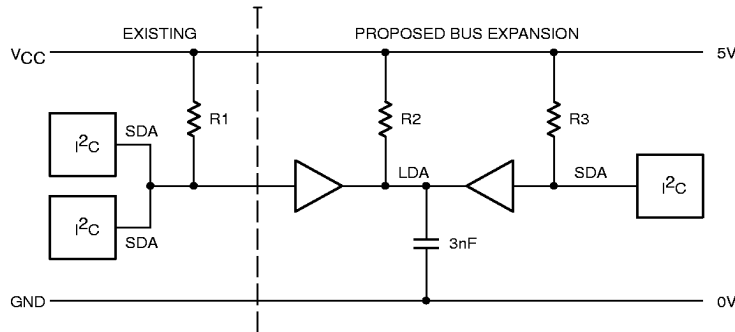
On the buffered low impedance line side, the corresponding output becomes LDA and LCL.

V_{CC}, GND — Positive and Negative Supply Pins

In normal use the power supply voltages at each end of the low impedance line should be comparable. If these differ by a significant amount, noise margin is sacrificed.

I²C bus extender

82B715



EFFECTIVE CAPACITANCE NEAR I²C DEVICES

2 × I ² C Devices	20pF
Strays	20pF
82B715 Buffer	10pF
TOTAL CAP.	50pF

I²C pull-up

$$R1 = \frac{1\ \mu\text{sec}}{50\text{pF}} = 20\text{K}\Omega$$

EFFECTIVE CAPACITANCE BUFFERED LINE

Wiring Cap.	3000pF
TOTAL CAP.	3000pF

Buffered Bus pull-up

$$R2 = \frac{1\ \mu\text{sec}}{3000\text{pF}} = 333\Omega$$

EFFECTIVE CAPACITANCE REMOTE I²C DEVICES

1 × I ² C Devices	10pF
Strays	10pF
82B715 Buffer	10pF
TOTAL CAP.	30pF

I²C pull-up

$$R3 = \frac{1\ \mu\text{sec}}{30\text{pF}} = 33\text{K}\Omega$$

AS AN ADDITION TO AN EXISTING SYSTEM * :

R1 = 20KΩ

$$R2 = \frac{R2 \times 0.1R3}{R2 + 0.1R3} = 300\Omega$$

R3 not required since buffer always connected

FOR A PERMANENT SYSTEM * :

R1 not required since buffer always connected

$$R2 = \frac{1}{\frac{1}{0.1R1} + \frac{1}{0.1R2} + \frac{1}{0.1R3}} = 262\Omega$$

R3 not required since buffer always connected

*** NOTE:**

R1, R2 and R3 are calculated from the capacitive loading and a 1μsec time constant on each bus node. For an addition to an existing system, R2' (the new value for R2) is shown as being calculated from the parallel combination of R2 and the scaled value of R3; while for a permanent system R2, and scaled values of R1 and R3 have been used. Note that this example has used scaled resistor values and combined the node and cable capacitances.

CHECK FOR MAXIMUM PULL-UP CURRENT:

$$\frac{(5 - 0.4)V}{260\Omega} = 17.6\text{mA} < 30\text{mA}$$

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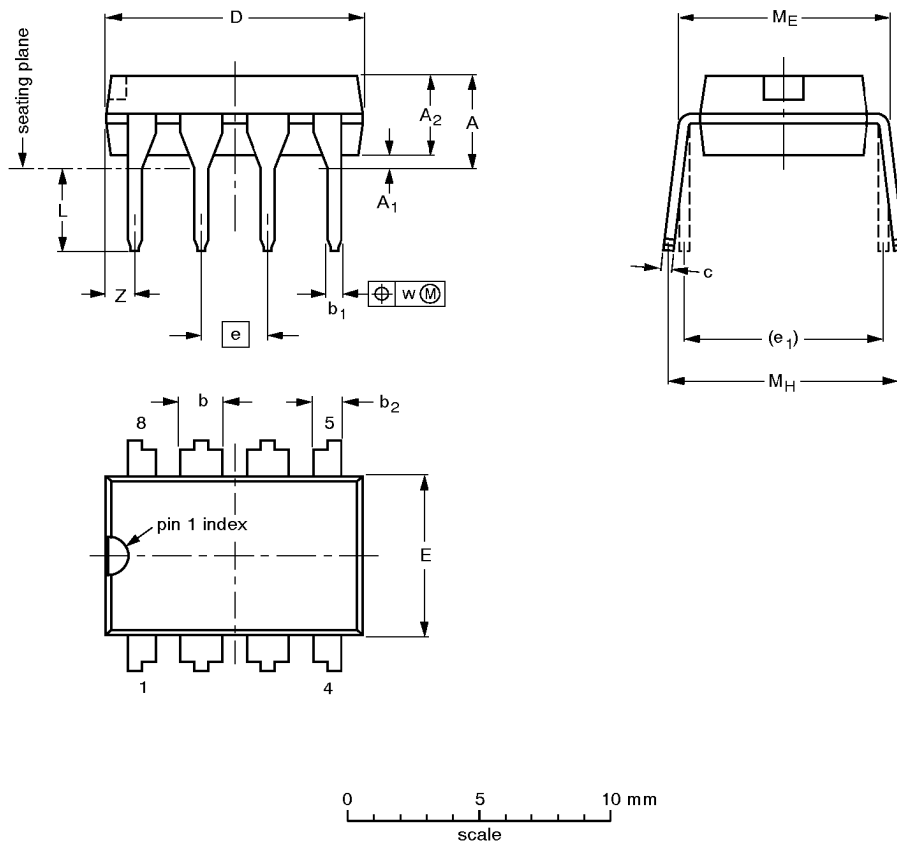
Figure 4. Typical Loading Calculation: I²C Bus with 82B715

I²C bus extender

82B715

DIP8: plastic dual in-line package; 8 leads (300 mil)

SOT97-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	b ₂	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

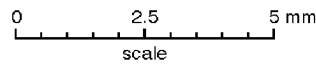
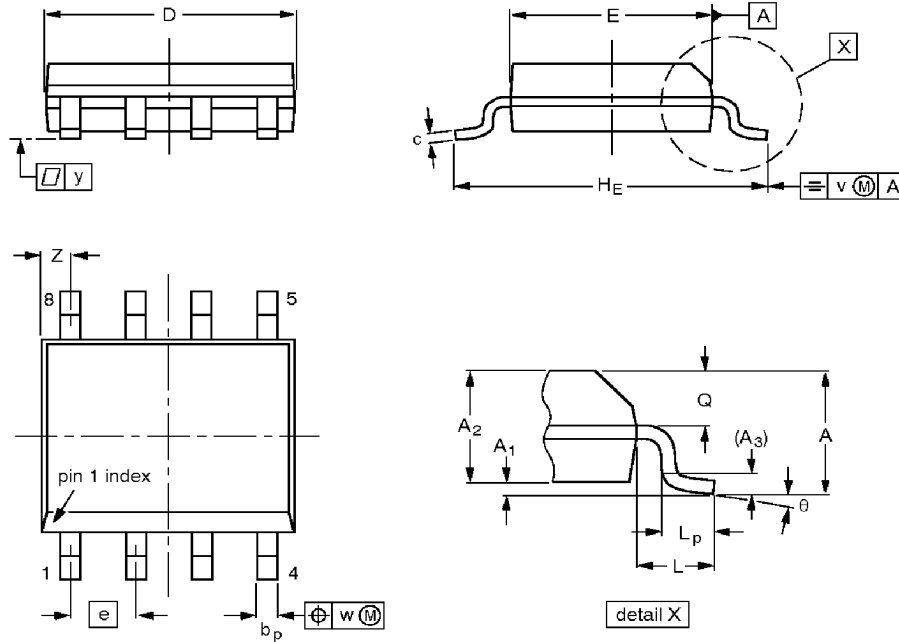
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001AN				92-11-17 95-02-04

I²C bus extender

82B715

SO8: plastic small outline package; 8 leads; body width 3.9mm

SOT96-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT96-1	076E03S	MS-012AA			95-02-04 97-05-22